

FIG

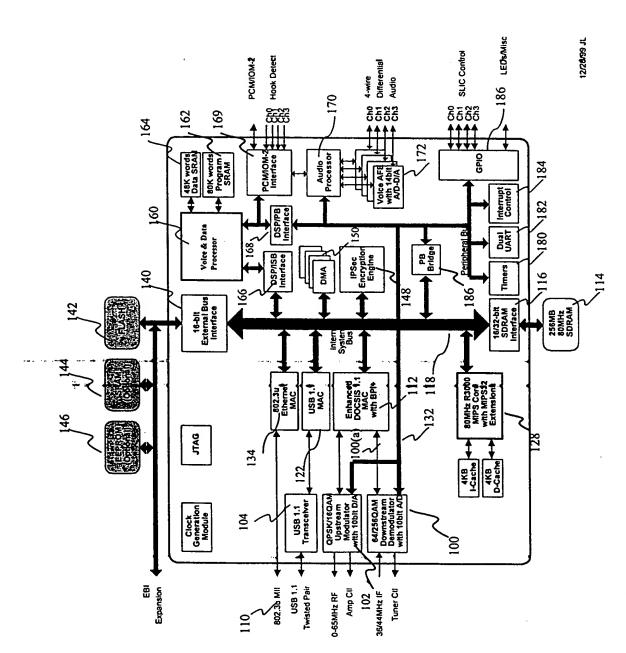
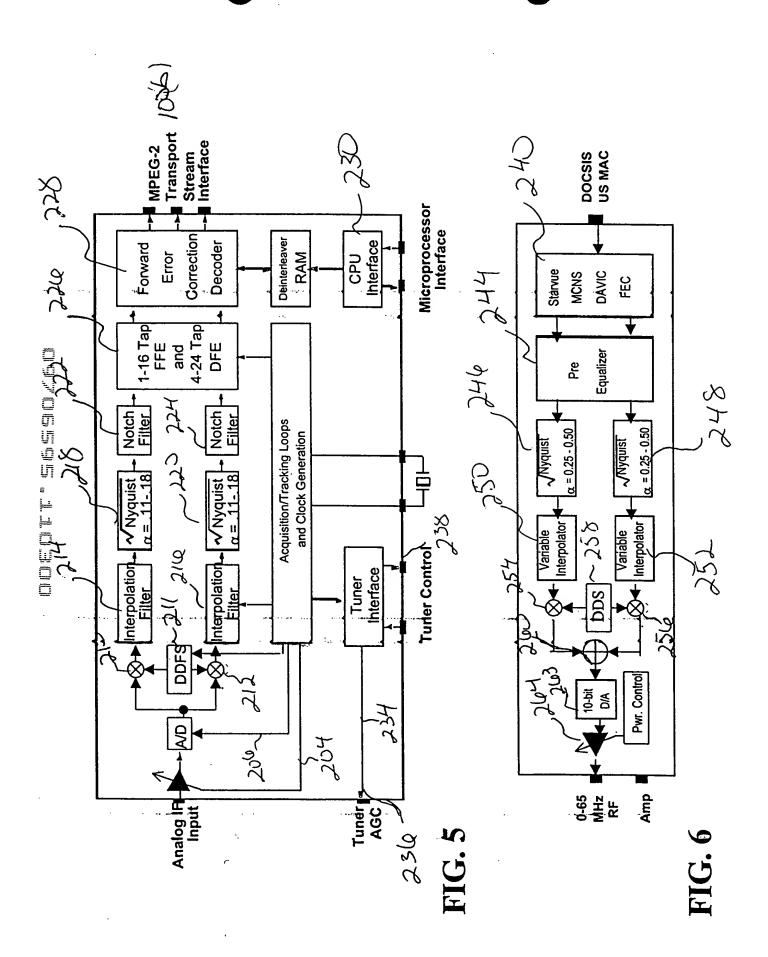


FIG. 3

**FIG.** 4



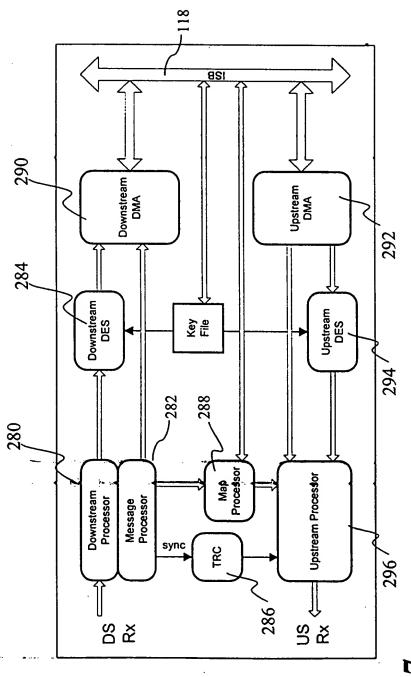


FIG.

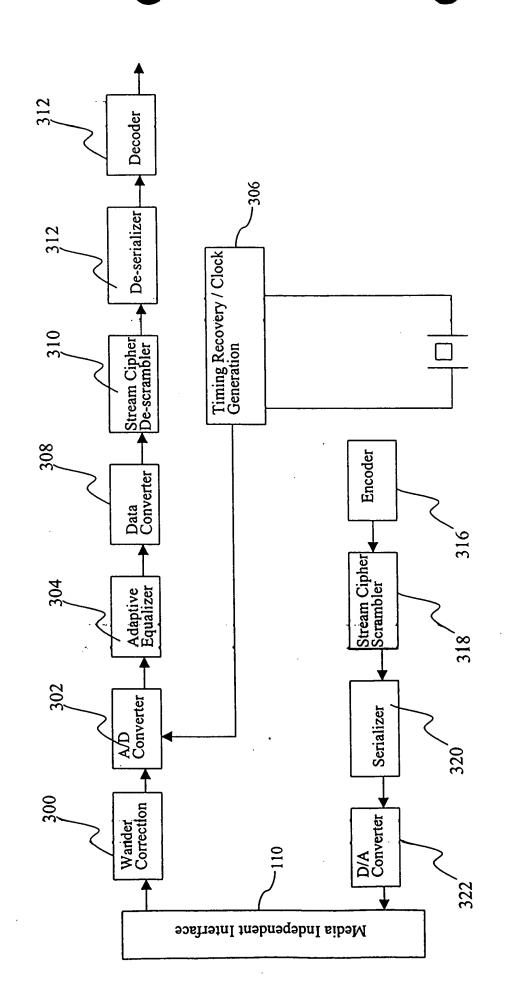


FIG. 8

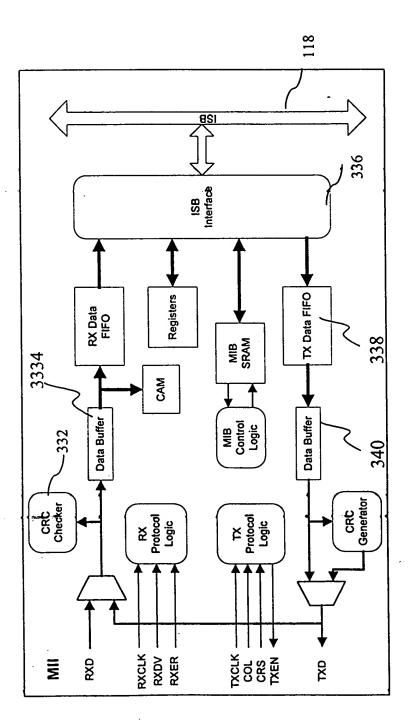
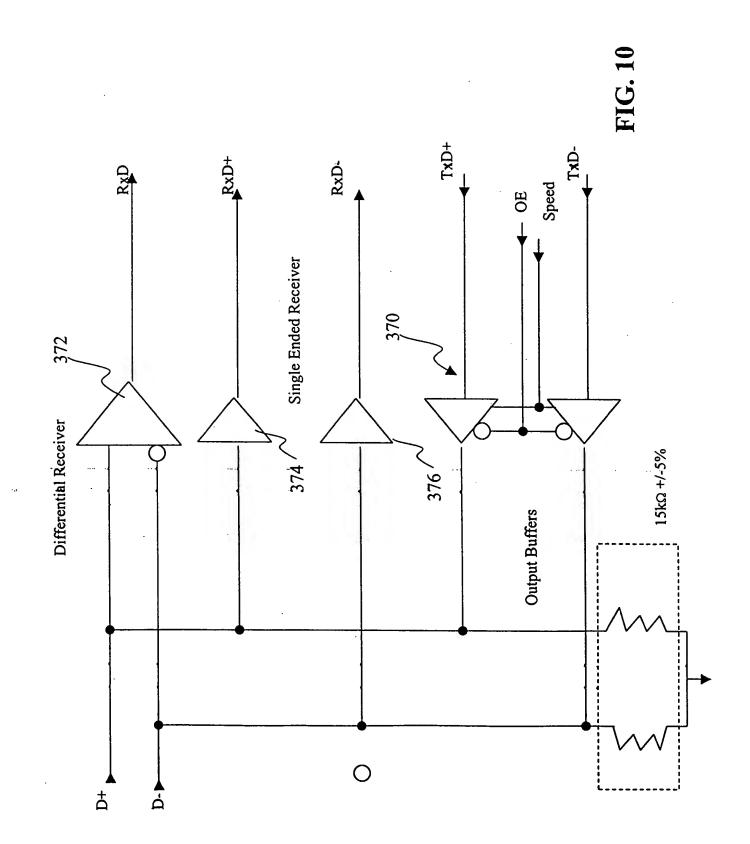
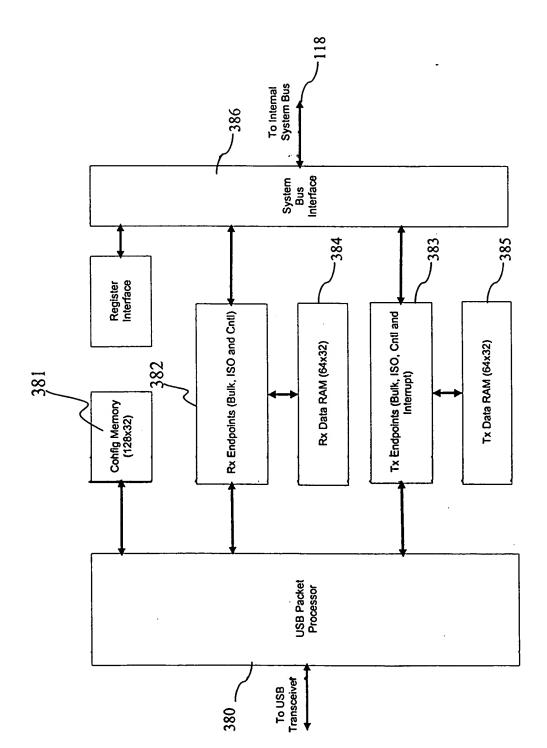
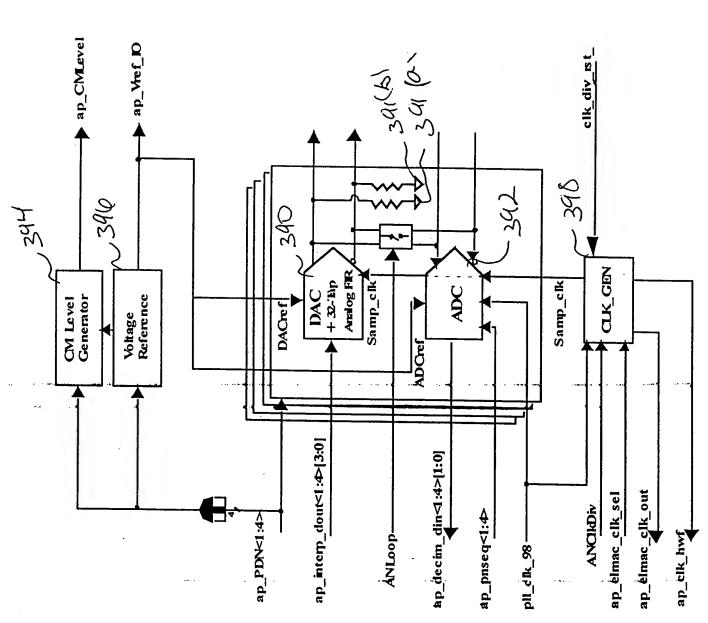


FIG.

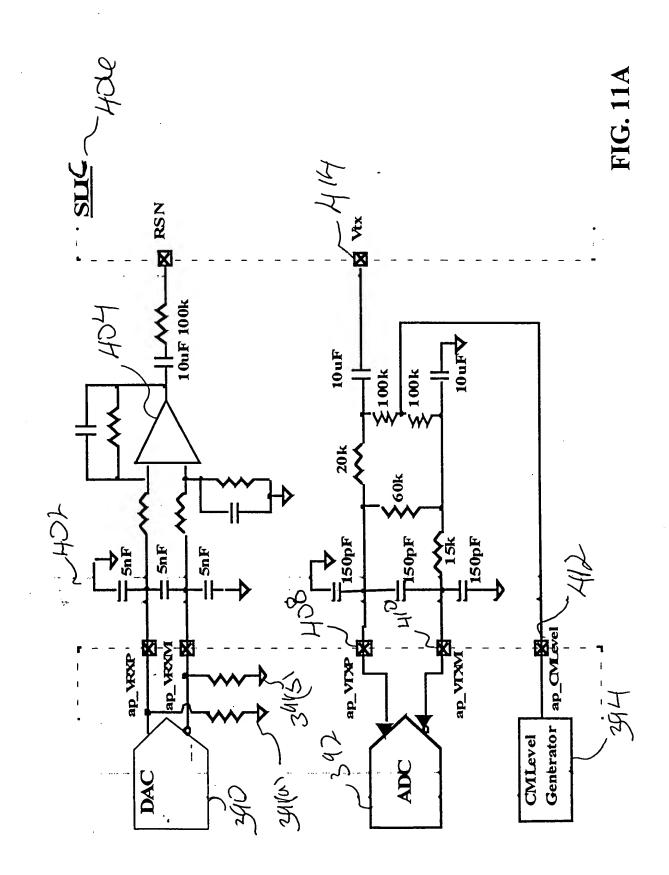




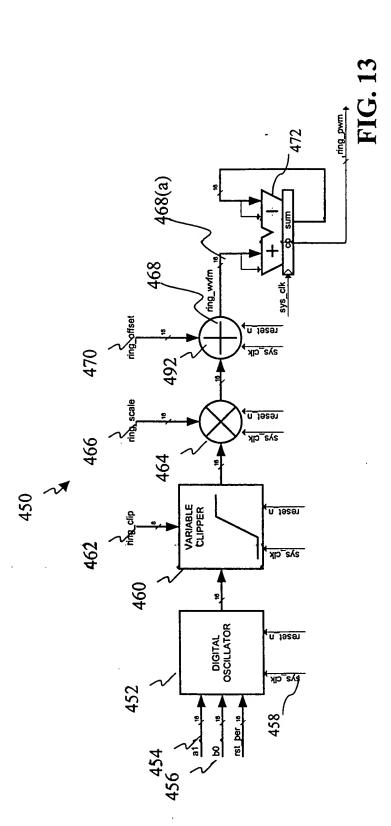
**FIG. 10A** 

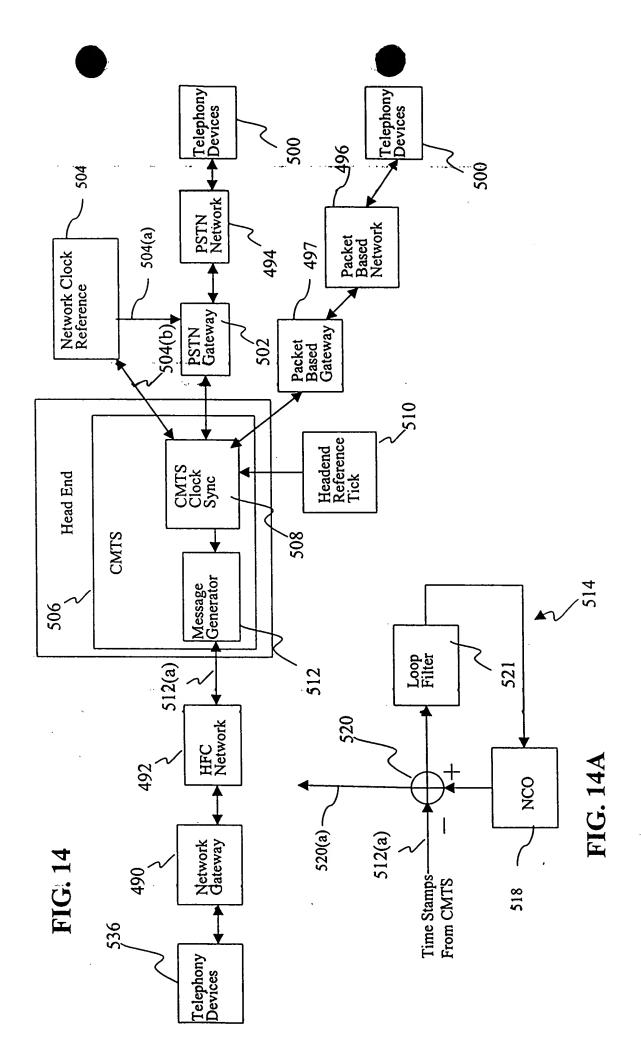


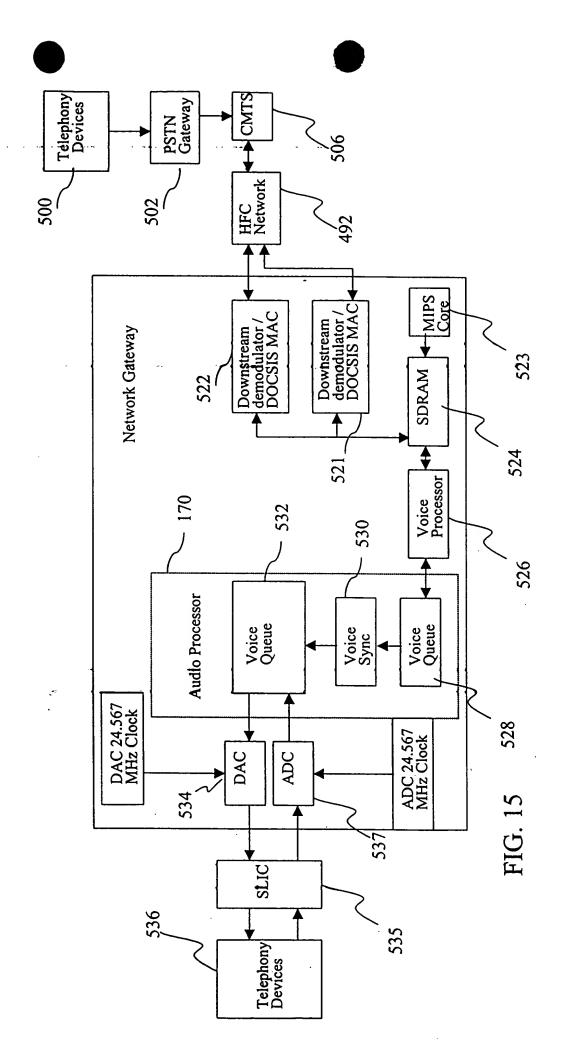
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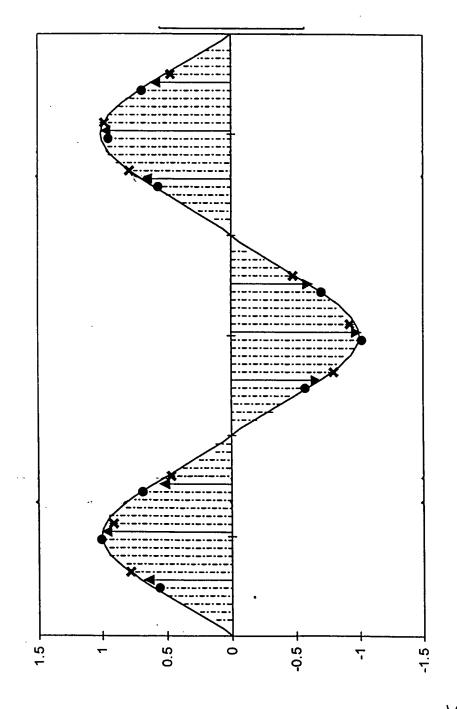
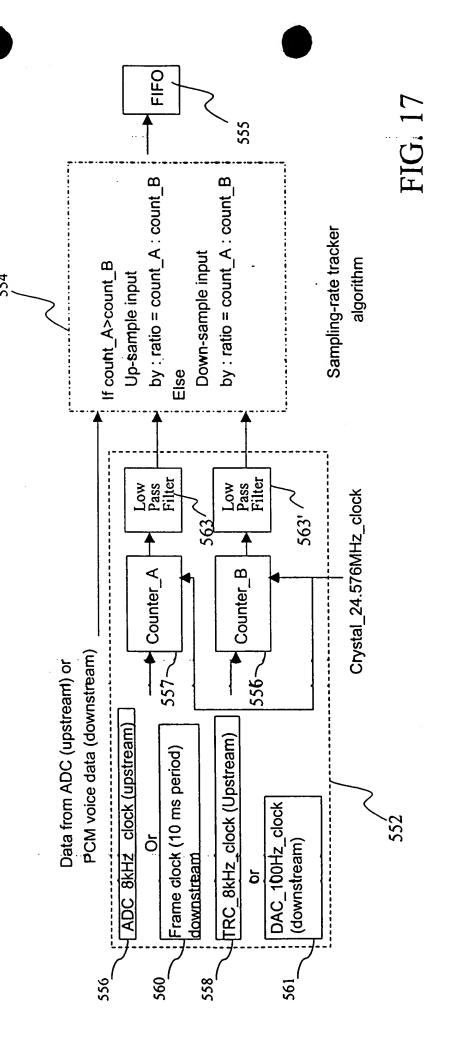


FIG. 16



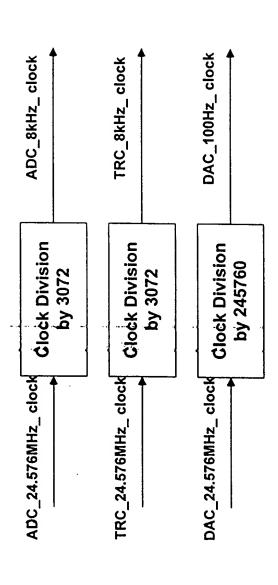
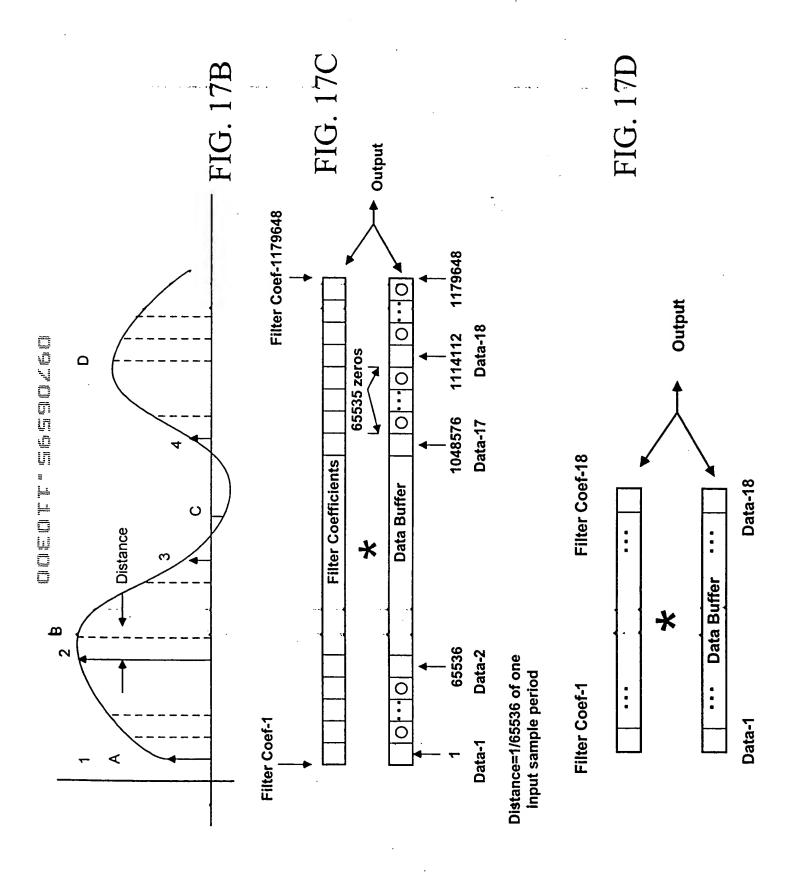
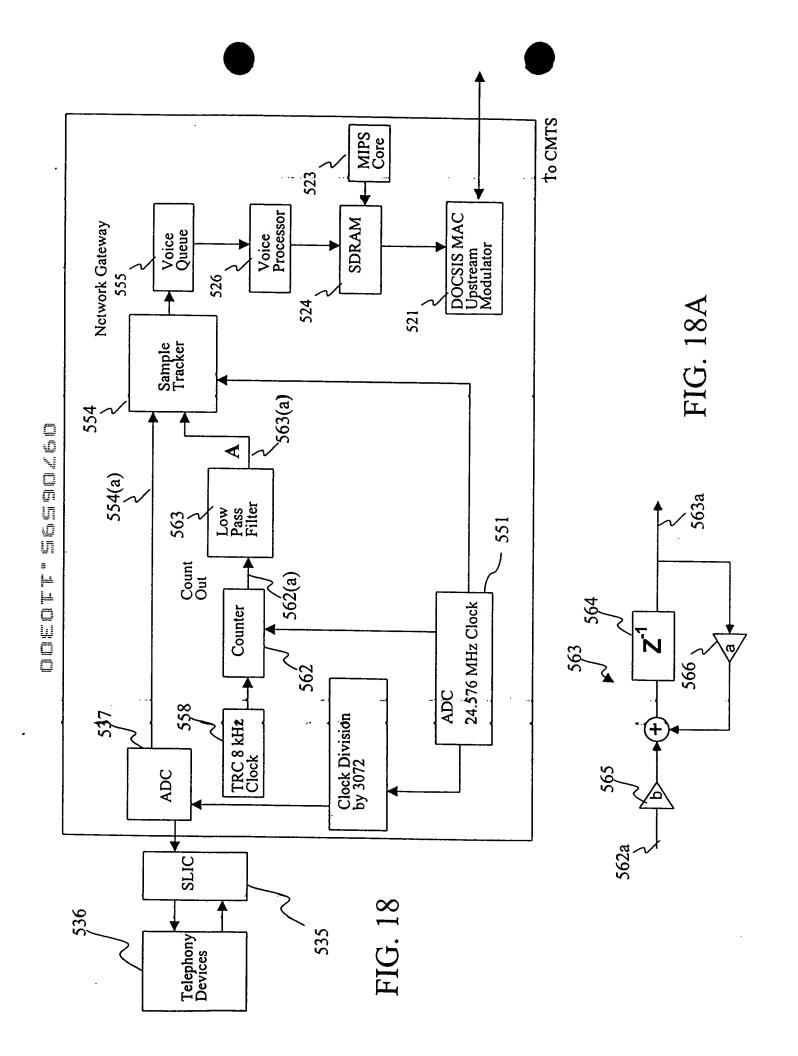
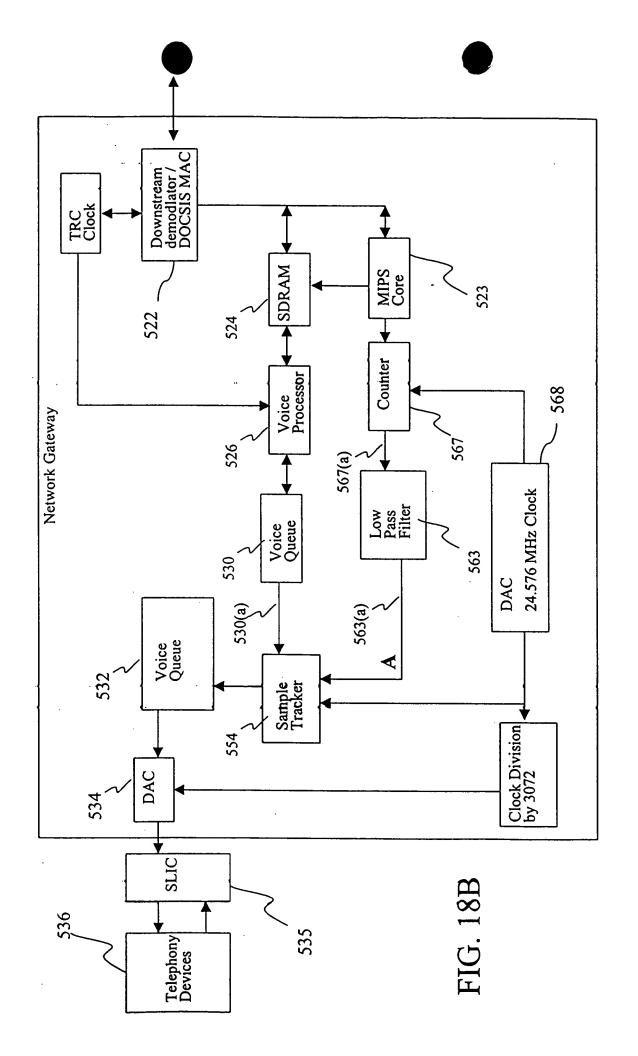


FIG. 17A







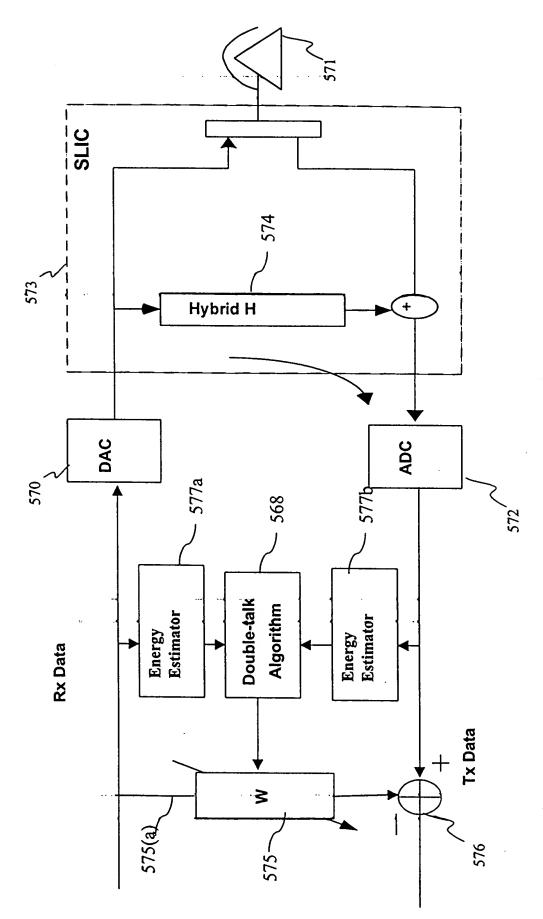


FIG. 19

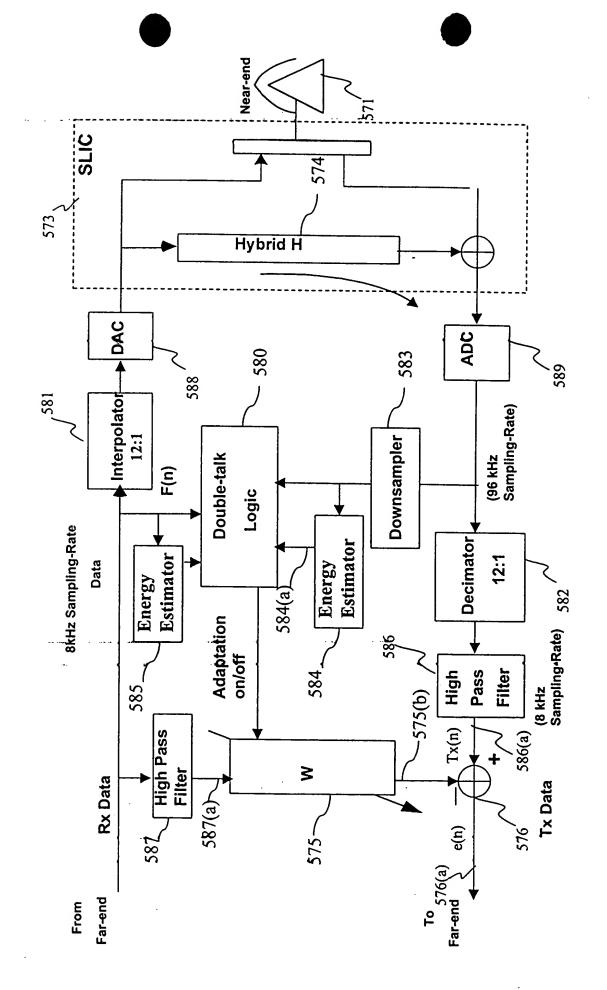


FIG. 20

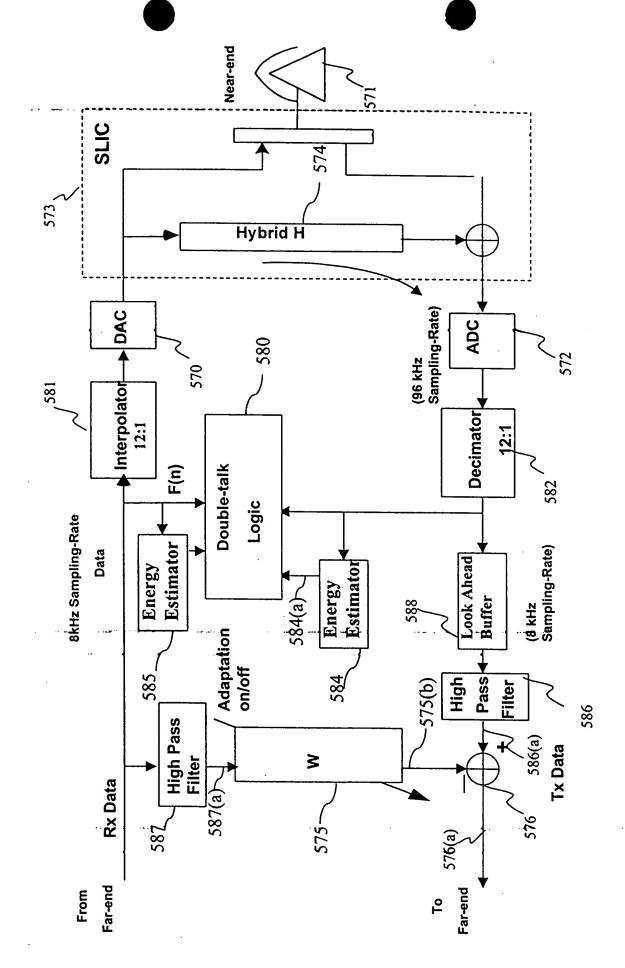
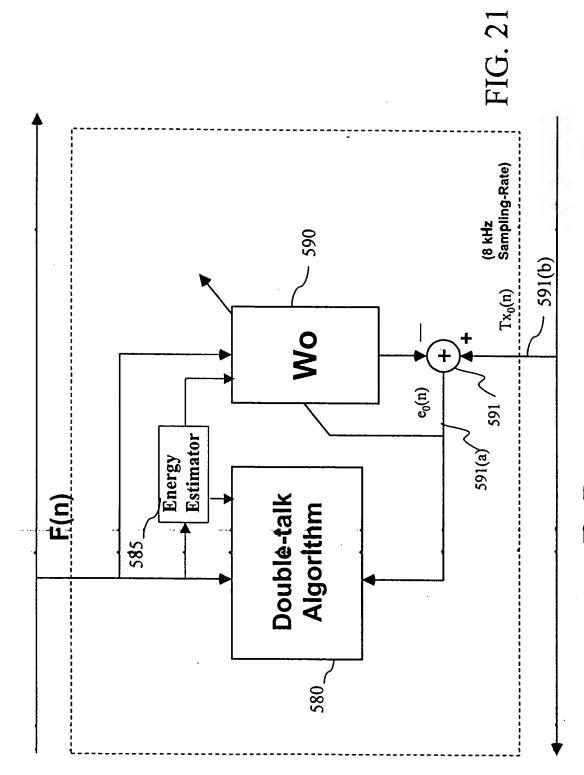
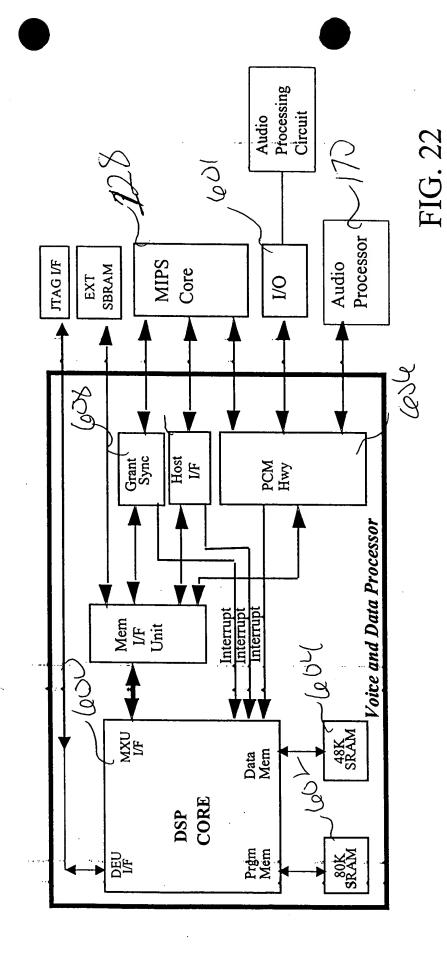
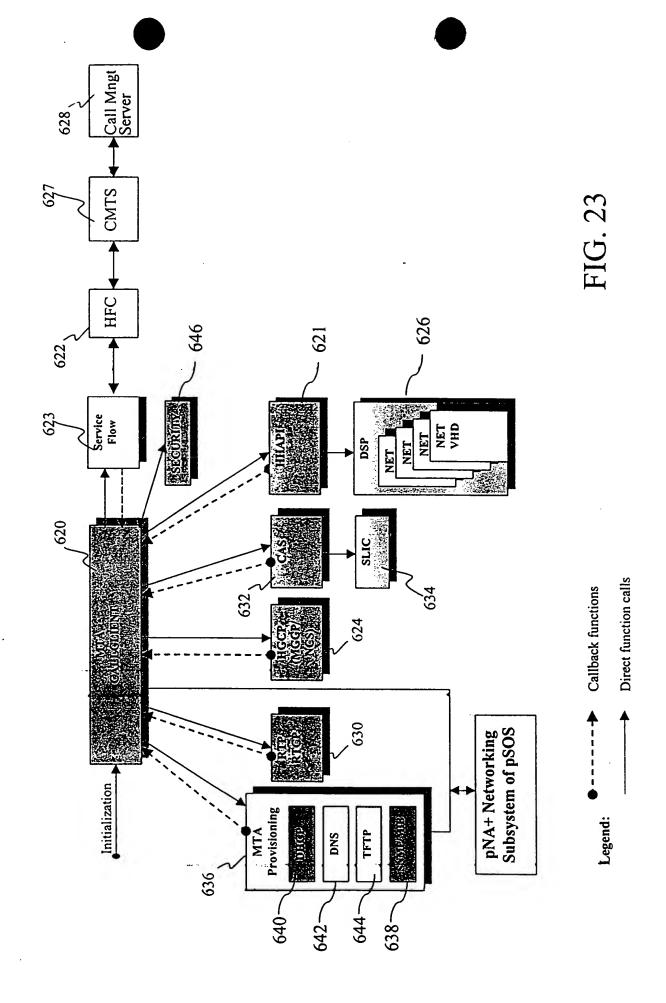


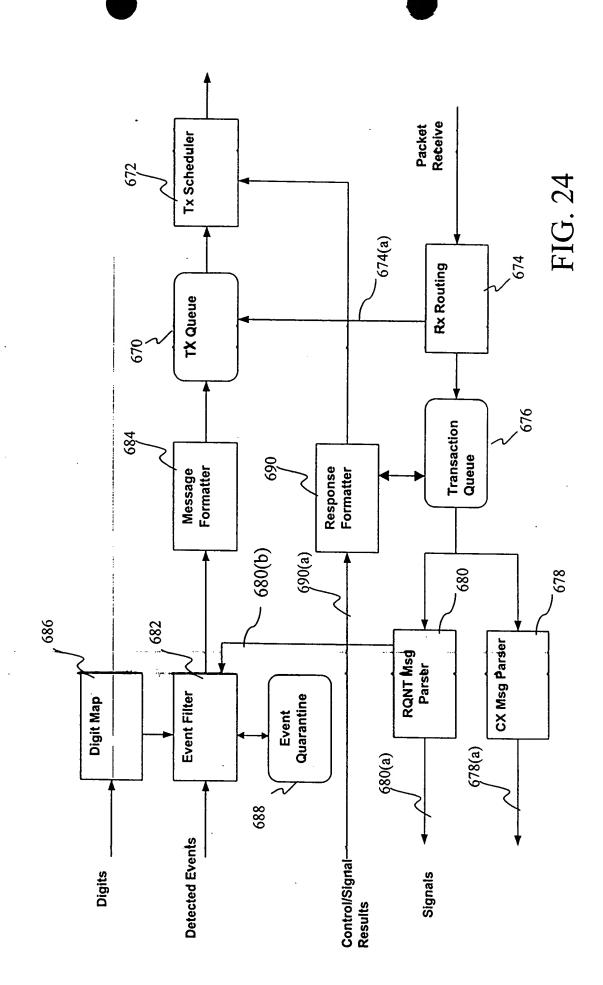
FIG. 20A



Tx Data







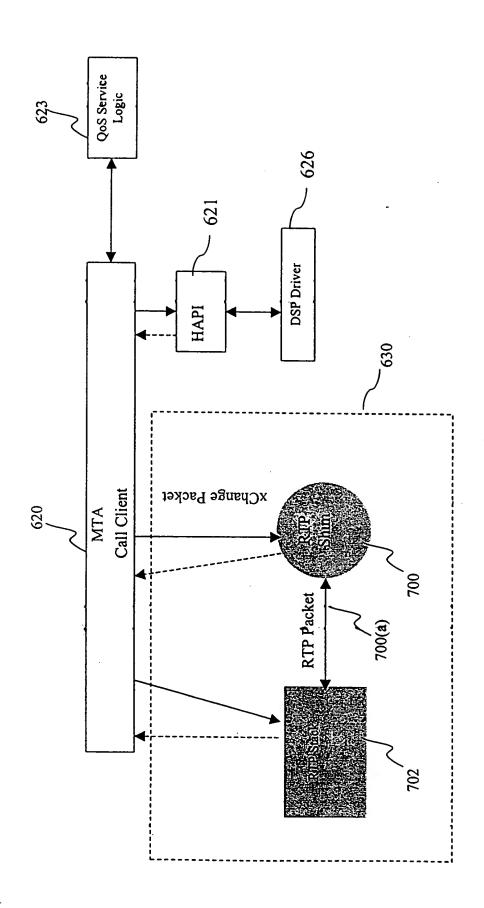


FIG. 25

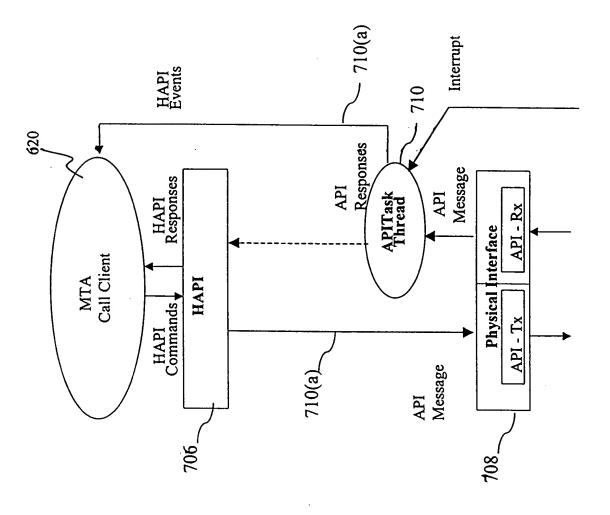


FIG. 26

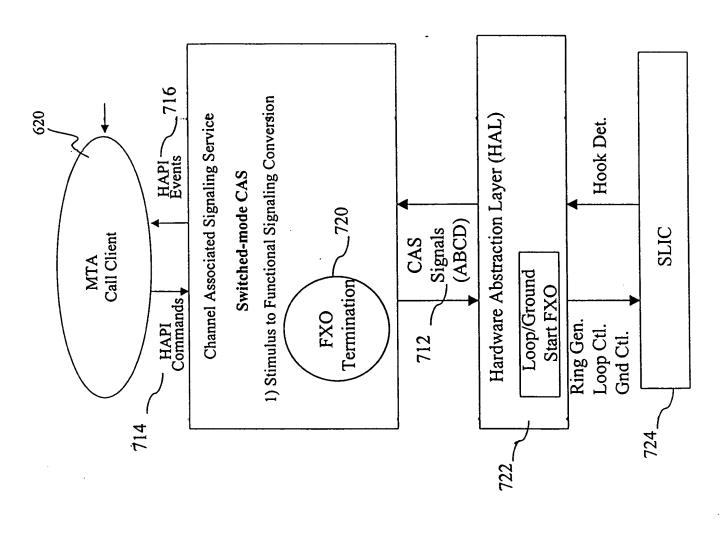
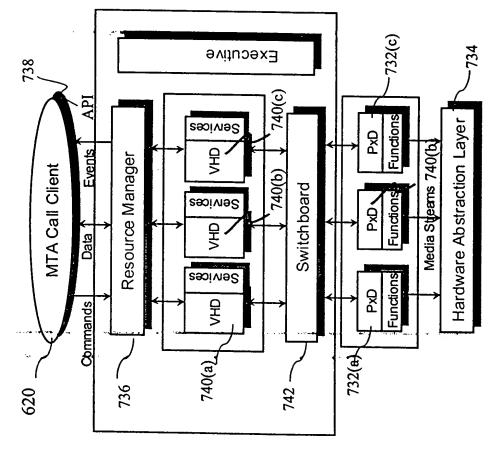


FIG. 27



To Underlying Hardware

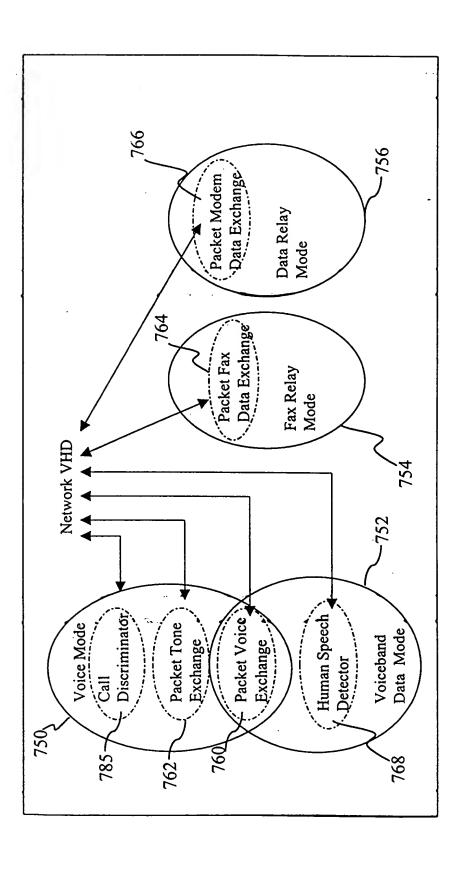
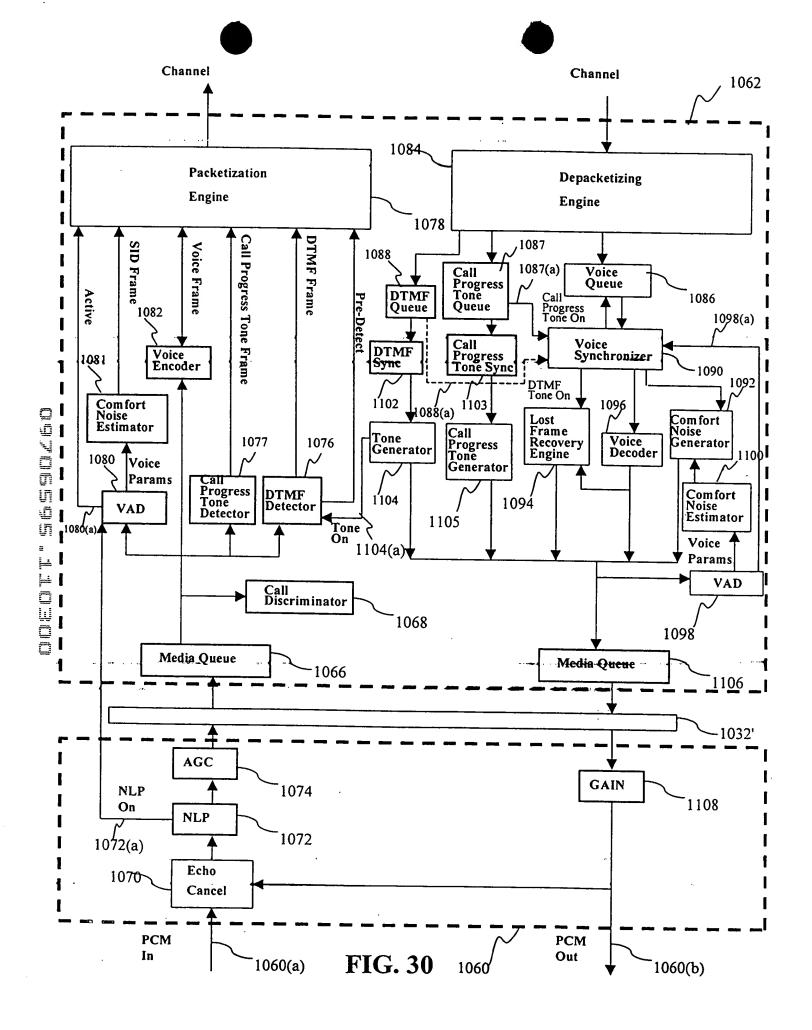
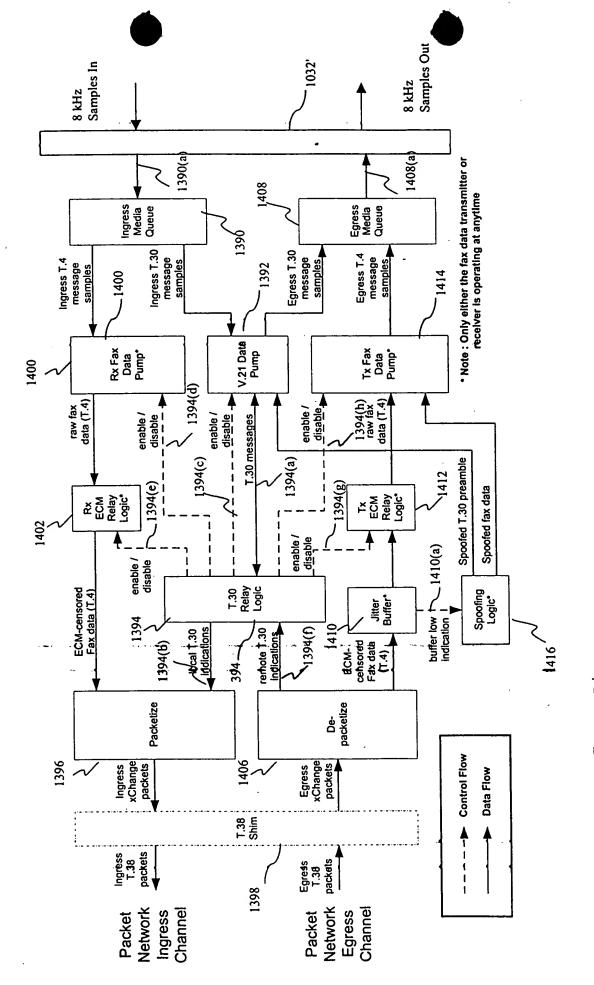
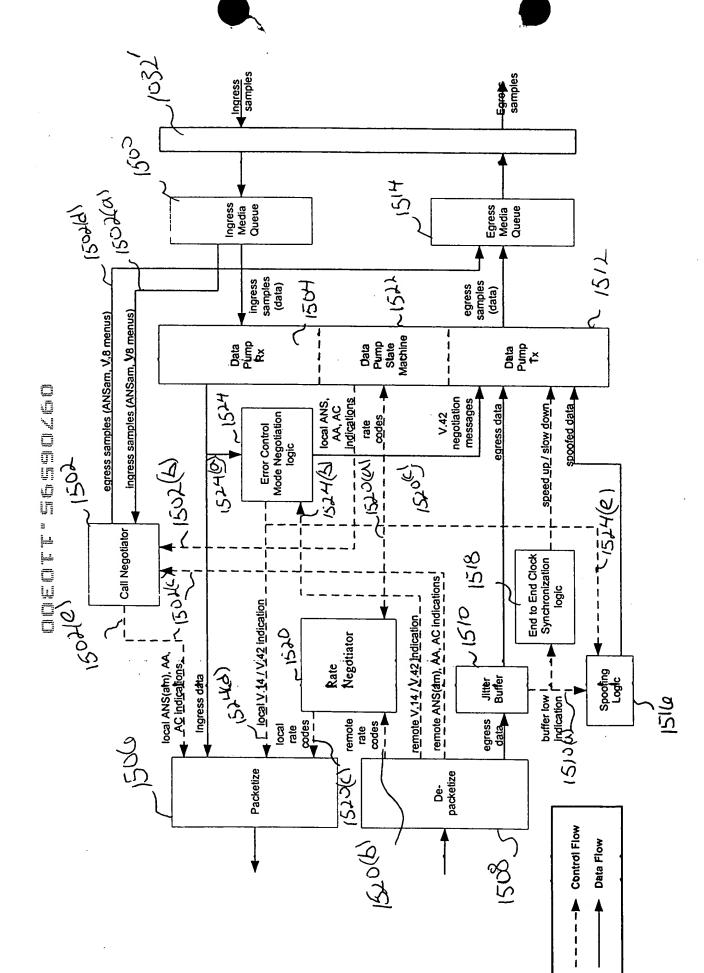


FIG. 29





F16.3



F16,32